REMARKS

1. In response to the final Office Action mailed September 11, 2007, Applicants respectfully request reconsideration. Claims 1, 2, 4-6, 8-20 and 22-31 were last presented for examination. Claims 3, 7 and 21 were previously canceled. By the foregoing Amendments, claims 1, 20 and 25 have been amended. Thus, upon entry of this paper, claims 1, 2, 4-6, 8-20 and 22-31 will remain pending in this application. Of these twenty-eight (28) claims, three (3) claims (claim 1, 20 and 25) are independent. Based on the above Amendments and the following Remarks, Applicants respectfully request that all outstanding objections and rejections be reconsidered, and that they be withdrawn.

Claim Rejections

2. In the outstanding Office Action, claims 1, 2, 4-6, 8-20 and 22-31 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over U.S. Patent No. 6,617,872 (hereinafter, "Vogley") in view of U.S Patent Application Publication No. US2003/0130969 (hereinafter, "Hawkins").

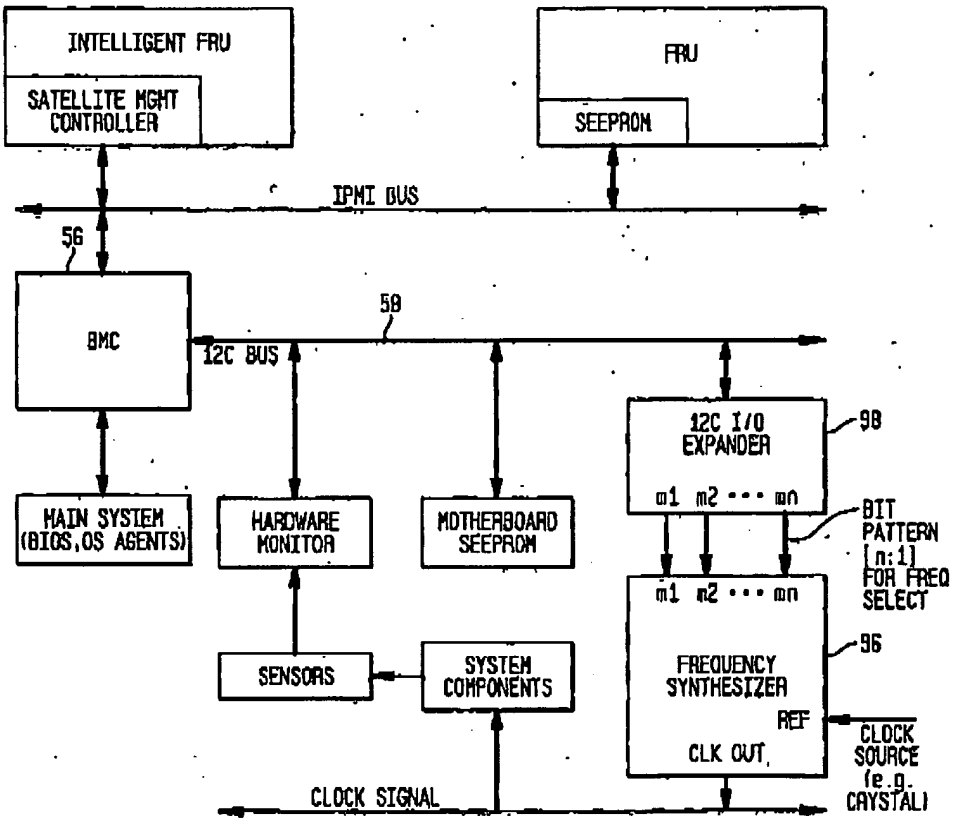
3. Claims 1, 20 and 25 have been amended to clarify the invention. In particular, claim 1 has been amended to recite:

> a baseboard management controller;
> an I^2C I/O expander configured to generate bit patterns in response to commands from said baseboard management controller; and
> a digital frequency synthesizer connected to the I^2C I/O expander by an I^2C I/O bus and configured to generate one or more test frequencies for application to one or more of a plurality of components of said electronic system in response to bit patterns generated by the I^2C I/O expander.

Claims 20 and 25 have been amended in a similar manner. Support for the amendments is provided by the original figures and specification. In particular, as shown in **FIG. 8** below and as the specification discloses, a baseboard management controller (BMC) employs a private I^2C (Inter-Integrated Circuit) bus **58** for communication with a hardware monitor and a motherboard

serial electrically erasable programmable read-only memory (SEEPROM) that contains information for the server's motherboard identification and further communicates with an Intelligent Platform Management bus(IPMB) in order to manage one or more field replaceable units (FRUs). More particularly, the BMC **56** can

FIG. 8



communicate with the frequency synthesizer **96** to vary its output clock frequency over a number of discrete values within a selected range and this variation of the output clock frequency can be utilized for frequency margin testing of the system components.

4. Further, as shown in **FIG. 8** and disclosed in the specification, an I^2C I/O expander **98** is *employed to supply a bit pattern of input signals to the synthesizer 96 in order to set the synthesizer's output clock frequency to a desired value and the BMC 56 communicates with the I^2C I/O expander, via the I^2C bus 58, to set values of selected output pins of the expander 98 to a desired bit pattern required to choose a synthesizer's output frequency of interest* (emphasis added). Therefore, it is respectfully submitted that the amendments raise no questions of new matter.

5. Vogley discloses an integrated circuit device test arrangement that includes a plurality of microcomputers where each of the microcomputers is interconnected directly through a separate test socket to a separate integrated circuit device that is inserted into the test socket.[1] In particular, as shown in **FIG. 1** below, Vogley discloses an integrated circuit device test arrangement **20** that includes integrated circuit devices **24, 25** which are plugged into or installed respectively in test sockets **30, 31**.[2] Further, Vogley discloses that the test sockets **30, 31** are mounted on one side of a test handler board **35** and on the other side of the test handler board **35**,

[1] Vogley at ABSTRACT.
[2] *Id.* at **FIG. 1**; and column 2, lines 57-60.

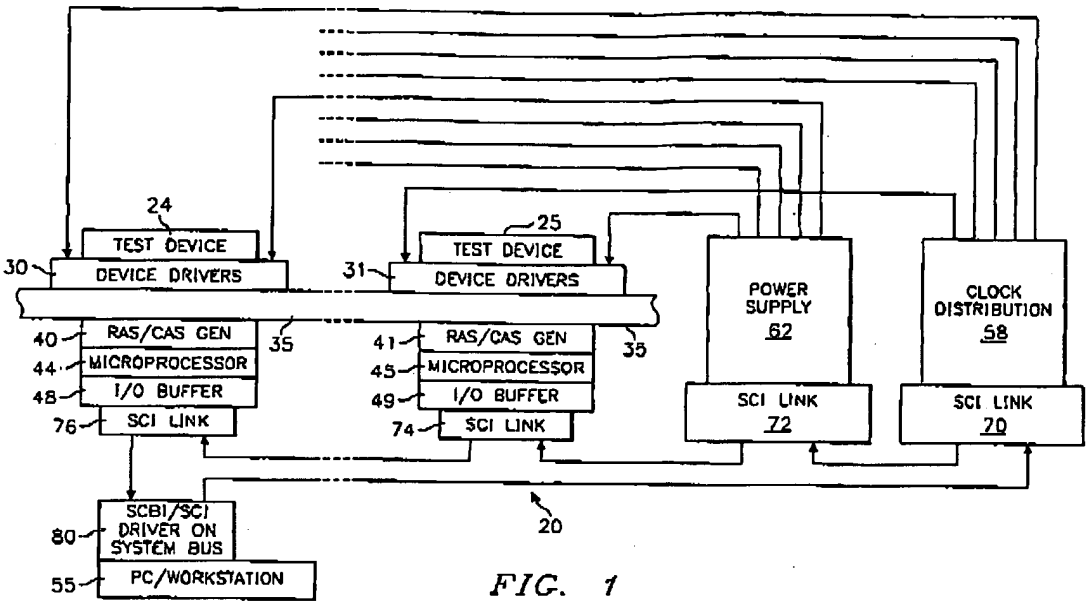


FIG. 1

there are microcomputer sockets **40, 41** into which are plugged, respectively, microcomputer devices **44, 45** with input/output buffers **48, 49**.[3] Further, Vogley discloses appropriate leads of the microcomputers **44, 45** are connected through the respective microcomputer sockets **40, 41**, and test sockets **30, 31** to the integrated circuit devices **24, 25**.[4]

6. In addition, Vogley discloses a personal computer or a workstation **55**, a clock distribution block **58**, a power supply **62**, scalable coherent interface (SCI) links **70, 72, 74, 76**, and an SCI driver arrangement **80**.[5] Furthermore, Vogley discloses a clock distribution block **58** applies clock signals by way of leads **85** to the test sockets **30, 31**; and power supply **62** supplies external voltages by way of leads **87** also to the test sockets **30, 31**.[6]

7. Moreover, Vogley discloses an exemplary test procedure (i.e., see **FIG. 2**) *controlled by the microprocessor associated with an individual integrated circuit device* (i.e., see **44, 45** in

[3] *Id.* at **FIG. 1**; and column 2, lines 60-64.
[4] *Id.* at **FIG. 1**; and column 2, lines 64 to column 3, line 1.
[5] *Id.* at **FIG. 1**; and column 3, lines 7-10.
[6] *Id.* at **FIG. 1**; and column 3, lines 13-16.

FIG. 1) is completed except for reporting resulting test data to the personal computer or work station (i.e., see **55** in **FIG. 1**; emphasis added).[7] That is, Vogley discloses microprocessors **44**, **45** set at least one operating parameter associated with at least one of said components to one or more test value in response to commands from the baseboard management controller (BMC).

8. However, Vogley nowhere discloses, as claim 1 recites:

> *an I^2C I/O expander configured to generate bit patterns in response to commands from said baseboard management controller;* and
> a digital frequency synthesizer *connected to the I^2C I/O expander by an I^2C I/O bus and* configured to generate one or more test frequencies for application to one or more of a plurality of components of said electronic system *in response to bit patterns generated by the I^2C I/O expander* (emphasis added).

That is, Vogley nowhere discloses as claim 1 recites:

(1) "an I^2C I/O expander configured to generate bit patterns in response to commands from said baseboard management controller;"
(2) "a digital frequency synthesizer connected to the I^2C I/O expander by an I^2C I/O bus;" and
(3) "bit patterns generated by the I^2C I/O expander." In addition, claims 20 and 25 recite similar limitations.

9. Thus, in consideration of the discussion above, it is respectfully submitted that Vogley does not disclose all of the limitations of independent claims 1, 20 and 25, and claims dependent thereon. Moreover, the outstanding Office Action acknowledges deficiencies of Vogley and attempts to overcome those deficiencies by combining Hawkins with Vogley. In particular, the outstanding Office Action states that Vogley: "does not specify that the microprocessor (i.e., controller) is a baseboard management controller," as recited in claim 1.[8] However, it is

[7] *Id.* at **FIG. 1**, **FIG. 2**; and column 4, lines 44-47.
[8] *Id.* at paragraph 3, page 3, lines 12-13.

respectfully submitted that Hawkins cannot overcome all of the deficiencies of Vogley, as discussed below.

10. Hawkins discloses a star Intelligent Platform Management Bus ("IPMB") topology that uses independent intelligent platform management buses between a central Baseboard Management Controller ("BMC") and various satellite management controllers ("SMCs")[9]. However, Hawkins nowhere discloses, as claim 1 recites:

> *an I^2C I/O expander configured to generate bit patterns in response to commands from said baseboard management controller;* and
>
> a digital frequency synthesizer *connected to the I^2C I/O expander by an I^2C I/O bus and* configured to generate one or more test frequencies for application to one or more of a plurality of components of said electronic system *in response to bit patterns generated by the I^2C I/O expander* (emphasis added).

That is, Hawkins nowhere discloses as claim 1 recites:

(1) "an I^2C I/O expander configured to generate bit patterns in response to commands from said baseboard management controller;"
(2) "a digital frequency synthesizer connected to the I^2C I/O expander by an I^2C I/O bus;" and
(3) "bit patterns generated by the I^2C I/O expander." In addition, claims 20 and 25 recite similar limitations.

Thus, Hawkins cannot overcome all of the deficiencies of Vogley. Therefore, it is respectfully submitted that neither Vogley nor Hawkins, whether taken alone or in combination, discloses, suggests or makes obvious the claimed invention and that claims 1, 20 and 25, and claims dependent thereon, patentably distinguish thereover.

[9] Hawkins at ABSTRACT.

Dependent Claims

11. The dependent claims incorporate all of the subject matter of their respective independent claims and add additional subject matter which makes them *a fortiori* independently patentable over the art of record. Accordingly, Applicants respectfully request that the outstanding rejections of the dependent claims be reconsidered and withdrawn.

Conclusion

12. In view of the foregoing, this application should be in condition for allowance. A notice to this effect is respectfully requested.

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Respectfully submitted,

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